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10/749,766	12/30/2003	Sang-Hoon Hong	51876P557	9102

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,766	HONG ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 30 December 2003 was fully considered by the examiner.

Drawings

3. The drawings were received on 30 December 2003. These drawings are deemed acceptable for examination.

Claim Objections

4. Claims 1-8 are objected to because of the following informalities:

As for claim 1, "a data" recited on line 8 of the claim (page 17) should be changed to "data". Additionally, "the predetermined cell block" recited on lines 11-12 (page 17) should be changed to "a predetermined cell block". Lastly, "the physical cell block address" recited on line 14 (page 17) should be changed to "the at least one physical cell block address".

As for claim 2, "an information" recited on lines 18-19 (page 17) should be changed to "information".

As for claim 3, "the physical cell block address" recited on line 4 (page 18) should be changed to "the at least one physical cell block address". Furthermore, "a data" as recited on line 26 (page 17) should be changed to "data".

As for claim 4, "the unit tag table" recited on line 2 of the claim (page 18) should be changed to "a unit tag table". Furthermore, "N number" on line 4 of the claim (page 18) should be changed to "N+1 number".

As for claim 5, "the candidate information" recited on line 21 (page 18) should be changed to "candidate information". Furthermore, "the logical cell block" recited on the very next line should be changed to "the logical cell block address".

As for claim 6, Examiner presumes Applicant intended claim 6 to depend on claim 4 directly for the following reasons: Claim 6 recites "third registers", however the first and second registers are not introduced until claim 4. Claim 6 further sets forth each third register as containing X+1 bits, however X is not defined as log base-2 of N until claim 4. The claim will further be treated on its merits based on the aforementioned presumption.

As for claim 7, "register" recited online 9 (page 19) should be changed to "registers". Furthermore, "register" recited online 13 (page 19) should be changed to "registers".

As for claim 8, the word "line" as recited online 26 (page 19) should be changed to "lines".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "the unit cell block" on lines 1-2 (page 18) of the claim. There is insufficient antecedent basis for this limitation in the claim, as it is unclear which of the plurality of unit cell blocks (as recited in claim 1) is being claimed. Applicant has further specified said cell block as the one with "a logical cell block address sensed by the row address", however Applicant fails to previously set forth the cell blocks as containing a *logical* cell block address (only provides for a *physical* cell block address).

Claim 7 recites the limitation "the selected unit cell block" on lines 15-16 (page 19) of the claim. There is insufficient antecedent basis for this limitation in the claim, as the claim fails to recite previously selecting a unit cell block. The claim will be further treated on its merits based on the presumption that "the selected unit cell block" is the cell block corresponding to the "at least one physical block address" as set forth in step (B) of the claim.

Claim 8 recites the limitation "the M number of third registers" on line 20 (page 19). There is insufficient antecedent basis for this limitation in the claim, as the claim fails to previously recite a third set of registers. The claim further recites "the predetermined cell block" on lines 20-21 (page 19). There is insufficient antecedent basis for this limitation in the claim as the claim fails to previously set forth predetermining a cell block among the plurality of cell blocks. The claim further recites, "the M number of predetermined word lines" on lines 21-22 (page 19). There is insufficient antecedent basis for this limitation in the claim, as the claim fails to previously set forth predetermining word lines.

Claims 4-6 are further rejected as they depend directly or indirectly on a previously rejected claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Burger et al., hereinafter Burger (US Patent 6,557,080 B1).

As for claim 1, Burger teaches a semiconductor device for refreshing data stored in a memory device, comprising:

a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be *any* positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of a cache memory;

a tag block having N+1 (in this example, 6) number of unit tag blocks, each storing at least one physical cell block address denoting a row address storing a data (Fig. 1, element 28) – col. 4, lines 48-62 – each tag block stores address information on each unit cell block (i.e. row of the cache memory) in order to execute address mapping; and

a control means (Fig. 1, element 18) for controlling the tag block and the predetermined cell block table (the cache control circuitry is used to control the subblock table (element 30) and the tag block (element 28)) and the for refreshing the data in the plurality of unit cells coupled to a word line in response to the physical cell block address (col. 3, line 66 through col. 4, line 5 – the control circuitry is used to refresh the cache) – The control circuitry uses the tag blocks and table to address the block or subblocks that require refreshing.

As for claim 2, Burger teaches the semiconductor device as recited in claim 1, further comprising:

a predetermined cell block table (Fig. 1, element 30) for storing an information representing at least more than one word line among the M number of the word lines storing data (the subblock table stores information for each subblock – col. 4, line 63 through col. 5, line 6). In other words, the table stores information, which includes as a whole, more than one word line among the M word lines, as each unit cell block contains one or more word lines. Even if any given unit cell block contains only one word line, the table still stores more than one word line as each of the plurality of unit blocks must contain at least one word line.

As for claim 7, Burger teaches a method for a refresh operation of a semiconductor memory device including a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be any positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of the cache memory; a tag block having N+1 (in this example, 6) number of unit tag blocks, each having M number of registers for sensing an update of data (col. 4, line 53 through col. 5, line 6) – each unit tag block holds information on each unit block (element 20) in a one-one correspondence. This information is used, among other things, to determine if data desired by the processor is still valid (i.e. requiring update/refresh or not), comprising the step of:

A) starting a refresh mode (refresh mode begins when the processor requests data. The data may then be refreshed if needed- col. 3, line 66 through col. 4, line 5 and col. 4, lines 63-67);

(B) finding at least one physical block address by decoding (N+1) X M number of second registers each storing logical block address (Fig. 2, element 30 depicts the subblock use table. The table stores information on each subblock contained in the cache col. 4, line 53 through col. 5, line 6 (each subblock has its own bit)). In other words the table contains a number of registers equal to the number of rows (i.e. N+1) times columns in the cache. The table is used to verify which data is valid (i.e. which will require updating or refreshing). Again there is a one-one correspondence for each entry in the table and the subblock within the cache, therefore the table is not only used to store the validity of the data, but can also be used to locate exactly which subblock to which its referring; and

(C) performing the refresh operation in the selected unit cell block (refresh is performed on the cache - col. 3, line 66 through col. 4, line 5). Again the cell, which is to be refreshed, must be selected (via the table) before the refresh operation can be performed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Burger as applied to claim 7 above, and in further view of Benedix et al., hereinafter Benedix (US PG Publication 2002/0141272 A1).

Examiner asserts that Burger in further view of Benedix renders claim 8 obvious based of the Examiner's best understanding of the claim in light of the ambiguities set forth under section 7 of this correspondence.

Though Burger teaches all the limitations of claim 7, he fails to disclose decoding registers in a cell block to find out which word line is respectively assigned to which cell block among the cell blocks, wherein the refresh operation is performed only on word lines not assigned as the M number of word lines.

Benedix however teaches a dynamic semiconductor memory with refresh and method for operating such a memory. In his disclosure, Benedix teaches in paragraph 0018 (all lines) memory cells disposed in rows and word lines. Further, the control device can selectively refresh word lines by resetting all of the word lines and only refreshing the selected ones. Further detail of the refresh operation is provided in paragraph 0020, lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Burger to further include Benedix's memory with refresh into his own cache with dynamic control sub-block fetching. By doing so, Burger would benefit by improving the refresh operation of his memory cells, hence improving

the overall memory access readiness of the memory as taught by Benedix in paragraph 007 (lines 1-9).

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

9. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-3, and 7-8 are provisionally rejected on the ground of nonstatutory double patenting over claim 42 of copending Application No.10/696,144 in further view of Burger and Benedix respectively. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

11. The subject matter claimed in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as follows:

Claim 1 of the instant application corresponds to (relevant sections of) claim 42 in the copending application as shown in the table below:

Claim 42: Copending Application 10/696,144	**Claim 1: Instant Application 10/749,766**
A memory device, comprising:	A *semiconductor* device *for refreshing data* stored in a memory device, comprising:
a cell area having N+1 number of unit cell blocks, each including M number of word lines	a cell area having N+1 number of unit cell blocks, each including M number of word lines *which respectively are coupled to a plurality of unit cells*;
a tag block for sensing an input logical cell block address for designating a unit cell block to be accessed to converting the input logical cell block address into a physical cell block address for designating a unit cell block to be restored in the row address;	a tag block *having N+1 number of unit tag blocks*, each storing at least one physical cell block address denoting a row address storing a data;
a control means for controlling the tag block and the predetermined cell block table for activating one word line of a unit cell block selected by the physical cell block address.	and a control means for controlling the tag block and the predetermined cell block table for *refreshing the data* in the plurality of unit cells coupled to a word line *in response* to the physical cell block address.

12. Though not all elements of the instant application are present in the copending application, the claim is rendered obvious in further view of Berger.

Claims 2-3, 7 (corresponding to Burger) and claim 8 (corresponding to Benedix) of the instant application are further rendered obvious as they correspond to claim 42 of the copending application, with the obvious variations to the claims supported by the cited art below.

As for claim 1, Burger teaches a semiconductor device for refreshing data stored in a memory device, comprising:

a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be any positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of the cache memory;

a tag block having N+1 (in this example, 6) number of unit tag blocks, each storing at least one physical cell block address denoting a row address storing a data (Fig. 1, element 28) – col. 4, lines 48-62 – each tag block stores address information on each unit cell block (i.e. row of the cache memory) in order to execute address mapping; and

a control means (Fig. 1, element 18) for controlling the tag block and the predetermined cell block table (the cache control circuitry is used to control the subblock table (element 30) and the tag blocks (element 28)) and the for

refreshing the data in the plurality of unit cells coupled to a word line in response to the physical cell block address (col. 3, line 66 through col. 4, line 5 – the control circuitry is used to refresh the cache) – The control circuitry uses the tag blocks and table to address the block or subblocks that require refreshing.

As for claim 2, Burger teaches the semiconductor device as recited in claim 1, further comprising:

a predetermined cell block table (Fig. 1, element 30) for storing an information representing at least more than one word line among the M number of the word lines storing data (the subblock table stores information for each subblock – col. 4, line 63 through col. 5, line 6). In other words, the table stores information, which includes as a whole, more than one word line among the M word lines, as each unit cell block contains one or more word lines. Even if each unit cell block contains only one word line, the table still stores more than one word line as each of the plurality of unit blocks must contain at least one word line.

As for claim 7, Burger teaches a method for a refresh operation of a semiconductor memory device including a cell area (Fig. 1, element 16) having N+1 number (in this example, 6) of unit cell blocks (element 20), each including M number of word lines which respectively are coupled to a plurality of unit cells (elements 24) – col. 4, lines 34-47. Note since the specification defines M as any positive integer, the number of word lines can be any positive integer. Though the word lines are not illustrated in Fig. 1, word lines are inherently part of the cache memory; a tag block

having N+1 (in this example, 6) number of unit tag blocks, each having M number of registers for sensing an update of data (col. 4, line 53 through col. 5, line 6) – each unit tag block holds information on each unit block (element 20) in a one-one correspondence. This information is used, among other things, to determine if data desired by the processor is still valid (i.e. requiring update/refresh or not), comprising the step of:

A) starting a refresh mode (refresh mode begins when the processor requests data. The data may then be refreshed if needed- col. 3, line 66 through col. 4, line 5 and col. 4, lines 63-67);

(B) finding at least one physical block address by decoding (N+1) X M number of second registers each storing logical block address (Fig. 2, element 30 depicts the subblock use table. The table stores information on each subblock contained in the cache col. 4, line 53 through col. 5, line 6 (each subblock has its own bit)). In other words the table contains a number of registers equal to the number of rows (i.e. N+1) times columns in the cache. The table is used to verify which data is valid (i.e. which will require updating or refreshing). Again there is a one-one correspondence for each entry in the table and the subblock within the cache, therefore the table is not only used to store the validity of the data, but can also be used to locate exactly which subblock to which its referring; and

(C) performing the refresh operation in the selected unit cell block (refresh is performed on the cache - col. 3, line 66 through col. 4, line 5). Again the cell, which is to be

refreshed, must be selected (via the table) before the refresh operation can be performed.

It would have been obvious to one of ordinary skill in art at the time of the invention for Ahn et al., hereinafter Ahn (US PG Publication 2004/085835 A1) – i.e. copending application - to further include Burger's cache with dynamic control of sub-block fetching. By doing so Ahn would benefit from Burger's system by providing a dynamically changing fetch block size for updating the cache based on statistical data as to how well a previous fetch block size was utilized by the processor as taught by Burger (col. 2, lines 35-41), thereby improving the overall cache efficiency with respect to cache misses as taught by Burger in col. 1, lines 59-67.

As for claim 8, Benedix teaches a dynamic semiconductor memory with refresh and method for operating such a memory. In his disclosure, Benedix teaches in paragraph 0018 (all lines) memory cells disposed in rows and word lines. Further, the control device can selectively refresh word lines by resetting all of the word lines and only refreshing the selected ones. Further detail of the refresh operation is provided in paragraph 0020, lines 1-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Ahn to further include Benedix's memory with memory device with reduced data access time. By doing so, Ahn would benefit by improving the refresh operation of his memory cells, hence improving the overall memory access readiness of the memory as taught by Benedix in paragraph 007 (lines 1-9).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Wang et al. (US Patent 6,697,909 B1) teaches a method and apparatus for performing data access and refresh operations in different sub-arrays of a DRAM cache memory.

Stracovsky et al. (US Patent 6,286,075 B1) teaches a method of speeding up access to a memory page using a number of M page tag registers to track a state of physical pages in a memory device having N memory banks were N is greater than M.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

2/20/08

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER